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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/619,478	07/19/2000	Shunpei Yamazaki	0756-2187	1882

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EXAMINER	
ANYASO, UCHENDU O	
ART UNIT	**PAPER NUMBER**
2675	25

DATE MAILED: 03/11/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/619,478	YAMAZAKI ET AL.	
	Examiner	Art Unit	
	Uchendu O Anyaso	2675	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. **Claims 1-32** are pending in this action.

Claim Rejections - 35 USC ' 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. **Claims 1, 2, 4-7, 9-18, 20-23, 25** and **26** are rejected under 35 U.S.C. 103(a) as being unpatentable over *Sawada* (U.S. 6,078,317) in view of *Kuwabara* (U.S. 6,507,332).

Regarding **independent Claims 1, 6, 11, 14, 17 and 22**, *Sawada* teaches a ferroelectric liquid crystal display (4) (column 3, lines 38-40, figure 1 at 4).

Furthermore, *Sawada* teaches an image signal processing circuit by teaching a video signal processor (2) and digital image processor (3) (column 3, lines 38-40, figure 1 at 2).

Also, *Sawada* teaches a control circuit in the form of a display mode dependence controller (17) that is connected to the digital image processor 3 and the scanning control circuit 22 (figure 1 at 3, 17). On the other hand, Sawada does not show the controller 17 feeding directly to display unit 4.

However, it would have been obvious to a person of ordinary skill in the art to learn from Sawada's design as to how to connect the controller 17 directly to the display unit 4 because the scanning control circuit 22 would be made an integral part of the display unit 4. [This

configuration resembles applicant's design which shows the control unit 170 connected directly to the source driver circuit 110, 120, and the gate driver circuit 130 (*see applicant's* figure 1 at 110, 120, 130).] The connection in Sawada of the controller 17 to the scanning control circuit 22 reads directly on applicant's circuit connectivity as shown in figure 1 (Compare figure 1 of Applicant and Sawada). The motivation for doing so would have been to provide a display device which can display an image in correspondence with various display modes (column 2, lines 40-45), and to achieve a scanning control circuit 22 that changes the scanning method in accordance with an instruction from the display mode dependence controller 17 in correspondence with the display mode (column 4, lines 40-43).

Furthermore, *Sawada* teaches that the gamma characteristic adjustment circuit (19) adjusts the characteristics included in the RGB image data in correspondence with the display panel (24) by utilizing a look-up table embedded within the gamma characteristic adjustment circuit (19) (column 4, lines 10-24, figure 1 at 19, 24).

However, Sawada does not teach explicitly a digital video signal dividing circuit. On the other hand, Kuwabara teaches a driving method for an active matrix type image display having a plurality of video signal lines wherein a scheme is designed to achieve a digital video dividing circuit of an original video signal (column 12, lines 10-27, figure 7).

Thus, it would have been obvious to a person of ordinary skill in the art to combine Sawada and Kuwabara's inventions because while Sawada teaches a method of controlling a display device with various display modes, Kuwabara teaches a method of driving the display device by using a video dividing scheme to prevent degradation in the display quality, and to reduce cost by simplifying the circuit construction (*see* column 12, lines 10-27, 61-67 through

column 13, line 4, figure 7). The motivation for doing so would have been to prevent degradation in the display quality column 12, lines 61-67 through column 13, line 4, figure 7).

Furthermore, Kuwabara teaches a gate driver 4, a source driver 3, and a digital video dividing circuit (see figure 9(a) at 3, 4, video1'-video4'). Also, Kuwabara teaches how the construction of the external circuits, such as video-signal forming circuits are optimized so as to fit the different scanning frequency, and the shared use of the substrate is available so that cost reduction is achieved (*see* column 4, lines 48-50; column 17, lines 42-63; Abstract).

Thus, it would have been obvious to a person of ordinary in the art to further optimize Kuwabara's invention by designing the video dividing circuit with the external circuits and then supplying the divided signals to other blocks of the display device. The motivation for doing so would have been to improve the reliability of the display device (column 17, lines 48-57).

Regarding **Claims 2, 5, 7, 10, 12, 13, 15, 16, 18, 21, 23** and **26**, in further discussion of claims 1, 6, 11, 14, 17 and 22, *Sawada* teaches a ferroelectric liquid crystal display (4) for a computer display (*see* column 3, lines 38-40, figure 1 at 4, *see also* column 1, lines 1-19).

Regarding **Claims 4, 9, 20** and **25**, in further discussion of claims 1 and 6, 17, 22, *Sawada* teaches circuitry wherein the video signal processor and the digital image processor contain the A/D conversion circuit (13) and the gamma characteristic adjustment circuit (19) respectively (column 3, lines 61-67 *through* column 4, lines 10-24 figure 1 at 13, 19).

Regarding **claims 27-32**, in further discussion of claims 1, 6, 11, 14, 17 and 22, *Sawada* teaches the controller 17 connected to the clock generator 14 (*see* figure 1 at 14, 17).

4. **Claims 3, 8, 19** and **24** are rejected under 35 U.S.C. 103(a) as being unpatentable over *Sawada* (U.S. 6,078,317) in view of *Kuwabara* (U.S. 6,507,332), as in claims 1, 6, 17 and 22 above, and further in view of *Jeong* (U.S. 6,008,801).

Regarding **Claims 3, 8, 19** and **24**, in further discussion of claims 1, 6, 17 and 22, *Sawada* and Kuwabara do not teach a source driver circuit with a D/A conversion circuit. On the other hand, *Jeong* teaches an invention related to a source driver for a thin film transistor liquid crystal display, which has a digital-to-analog converter (column 1, lines 10-14).

Thus, it would have been obvious for a person of ordinary skill in the art to combine Sawada, Kuwabara and *Jeong's* inventions because while the combination of *Sawada* and Kuwabara teach a driving method for an image display having a plurality of video signal lines wherein a scheme is designed to achieve a digital video dividing circuit of an original video signal, *Jeong* teaches a source driver for a thin film transistor liquid crystal display which has a digital-to-analog converter. The motivation for combining these inventions would have been to reduce the power consumption of the source driver, and thus, reduce the power consumption of the liquid crystal device (column 4, lines 1-5).

Response to Arguments

5. Applicant's arguments filed February 23, 2004 have been fully considered but they are not persuasive.

Applicant amended independent claims 1, 6, 11, 14, 17, and 22 to include the feature that the control circuit directly feeds pulses to an image signal processing circuit, a digital video dividing circuit, a source driver circuit, and a gate driver circuit. On this issue, applicant seems to be exploring novelty by honing in on connectivity. However, it has clearly been shown in the rejection above the rationale and motivation for combining Sawada and Kuwabara in order to accomplish applicant's invention. That is, Sawada teaches a control circuit in the form of a display mode dependence controller (17) that is connected to the digital image processor 3 and the scanning control circuit 22 (figure 1 at 3, 17). Furthermore, Kuwabara teaches a gate driver 4, a source driver 3, and a digital video dividing circuit (see figure 9(a) at 3, 4, video1'-video4'). Specifically, while Sawada does not teach explicitly a digital video signal dividing circuit, Kuwabara teaches a driving method for an active matrix type image display having a plurality of video signal lines wherein a scheme is designed to achieve a digital video dividing circuit of an original video signal (column 12, lines 10-27, figure 7). Thus, it would have been obvious to a person of ordinary skill in the art to combine Sawada and Kuwabara's inventions because while Sawada teaches a method of controlling a display device with various display modes, Kuwabara teaches a method of driving the display device by using a video dividing scheme to prevent degradation in the display quality, and to reduce cost by simplifying the circuit construction (*see* column 12, lines 10-27, 61-67 through column 13, line 4, figure 7). The motivation for doing so would have been to prevent degradation in the display quality column 12, lines 61-67 through column 13, line 4, figure 7).

Applicant further asserts that the digital video dividing circuit is formed within the source driver as opposed to being formed individually. On this issue, applicant should note that

Kuwabara teaches a gate driver 4, a source driver 3, and a digital video dividing circuit (see figure 9(a) at 3, 4, video1'-video4'). Also, Kuwabara teaches how the construction of the external circuits, such as video-signal forming circuits is optimized so as to fit the different scanning frequency (*see* column 4, lines 48-50; column 17, lines 42-63; Abstract). Thus, it would have been obvious to a person of ordinary in the art to further optimize Kuwabara's invention by designing the video dividing circuit with the external circuits and then supplying the divided signals to other blocks of the display device (column 17, lines 42-63). The motivation for doing so would have been to improve the reliability of the display device (column 17, lines 48-57).

As such, applicant's amendments and arguments are not persuasive.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent 6,025,835 to *Aoki et al* for a driving circuit for display apparatus with paired S/H circuits.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Uchendu O. Anyaso whose telephone number is (703) 306-5934. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steve Saras, can be reached at (703) 305-9720.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

Uchendu O. Anyaso

03/06/2004

CHANH NGUYEN
PRIMARY EXAMINER